Main Directions of Riga Event Timer Development and Current Results

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ABSTRACT

The present-day high-performance event timers (including Riga event timers) already offer the resolution and measurement speed that are quite enough for Satellite Laser Ranging applications. Taking that into account, currently we focus our research activity on the compact design and advancing of other important performance characteristics of Riga Event Timers, such as their reliability, friendliness, hardware simplicity, affordable price, etc. In this report we present current results of such activity and suppose that a next model of Riga event timer could be offered already in the nearest future to cover a wider range of applications (including airborne ones).

Introduction

The Riga event timers represent computer-based instruments that measure time instants when input events (represented by NIM logic pulses) occur. Distinguishing feature of these instruments is a high precision combined with a high measurement rate due to the innovative DSP-based technology for event timing [*Artyukh Yu,* 2001]. In particular, the latest model A033-ET of the Riga event timers offers single-shot RMS resolution better than 5 ps and measurement rate up to 20 MHz, making this instrument one of a few best event timers currently available [*Artyukh Yu.*, *et al.,* 2011]. Combining the A033-ET with application-specific software, a number of top-quality and reasonably priced event timer systems can be created. But there are some essential characteristics, which can be improved to provide the SLR users with more reliable, simplified and friendly device retaining the precision and performance of the A033-ET.

We are working on three main directions of Riga Event Timer (ET) project advancing:

1. Supporting of stable repeatability of the precision at the level 3 ps RMS in a wide temperature range by means that include:
    - temperature stabilization of the main measurement node,
    - temperature compensation schematic,
    - more robust and timekeeping calibration procedure;.
2. More compact design and faster operating by the means that include:
    - integration of all digital functions in single FPGA of the timer's hardware,
    - higher clock frequency (considerably more that the previously used 100 MHz),
    - higher-speed PC interfaces, such as USB3, PCIe, Ethernet 1G, etc;
3. User interface friendliness including integration and simplification of user-initiated function on PC.

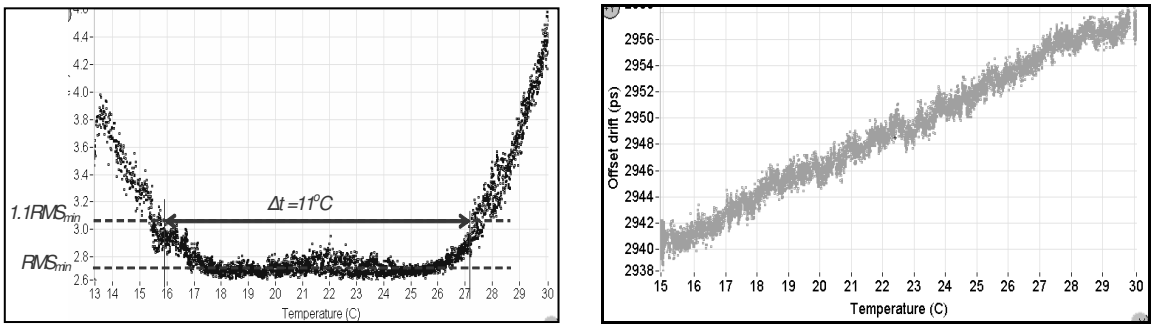
The state of these directions and their evolution will be considered below in more detail.

1 The best and stable precision

The main factor impacting on Riga ET measurement precision is a temperature variation. Due to the environment temperature variation all electronic components of the timer's hardware change their characteristics. As a result, the transfer function, describing the event-to-time conversion, slightly changes, too. At the beginning of the A033-ET development the single-shot RMS resolution degradation by more than 10 percent occurred beyond the range of calibration temperature ±3 ^{o}C. We thought it would be enough for effectively employing a thermostat. For this reason firstly we have made some

experiments with a placement of the measurement node into a self-made small thermostat. Our experiments showed that neither thermostat with heating elements nor thermostat with cooling on the base of Peltier elements could not provide a sufficient precision stability and were not the best solution in terms of the hardware simplicity, compactness and power consuming.

Therefore other solutions of the problem were investigated. Unlike the temperature stabilization, right temperature compensation, where it is possible, leads to a sufficiently effective solution. In the latest versions of the A033-ET such temperature compensation is applied for both precision stabilization and decreasing the single-input offset drift [*Artyukh Yu., et al., 2011*]. The last parameter seems most essential in the tasks related with one-way laser ranging and time transfer experiments. Temperature dependences typical for the A033-ET precision and epoch offset are presented in Figure 1.



a) **b)**

Figure 1. Temperature impact on A033-ET performance: a) precision degradation; b) single-input offset drift

One can see in Figure 1a, that, as the result of temperature compensation, temperature range is considerably expanded around the temperature when the device calibration has been performed. In this case the single-shot RMS resolution degradation by more than 10 percent occurs beyond the range of 11 ^{o}C. Such compensation also decreases the single-input offset drift and, as can be seen from Figure 1b, this drift is only a little greater than 1 ps/ ^{o}C.

In the case of essential temperature change there is no possibility to compensate electronic component parameters drift without traditional calibration procedure. The calibration procedure includes calculating a new, more adequate, transfer function in accordance with the current ambient environment. In Riga ET the calibration procedure is executed using a dedicated signal, which is produced by a generator embedded into Riga ET hardware. The problem occurs when this generator frequency is out of the range of frequencies, which are the best for calibration. For example, as a result of frequency deviation in full working temperature range 0 – 50 ^{o}C, there can appear the frequencies, which give very bad calibration results (increasing the single-shot RMS resolution up to 100 ps!). In other words, such “bad frequencies” are unacceptable for calibration procedure.

Currently this problem is solved by means of switching the embedded generator between two adjacent frequencies, differing by only about 0.3 ppm. A choice between these frequencies is done on the base of specially developed estimate of the frequency “badness”. From two adjacent frequencies the frequency with the lower estimate is chosen. This approach allows providing the required resolution “almost always”.

Another approach to solve this problem lies in stabilizing the selected frequency and keeping it in a narrow range of the best frequencies for calibration. The first experiments with Frequency-Locked Loop (FLL) and Phase-Locked Loop (PLL) solutions for optimal frequency synthesis showed the effectiveness of such approach. In this case every new calibration always allows to get the RMS resolution for the single-shot interval measurement at the lowest limit in a wide temperature range (figure 2).

Both FLL and PLL synthesizers give the good results independent on a temperature variation. Theoretical basis and practice for PLL generator implementations is well developed, and there are some specialized chips which are ready to use. PLL synthesizer is more suitable for very stable frequency retention, but in off-the-shelf devices there are restrictions in an output frequency choice. FLL synthesizer can be oriented to the slight frequency adjusting but has more complicated retention mechanism, but in case of large FPGA using this is not a problem.

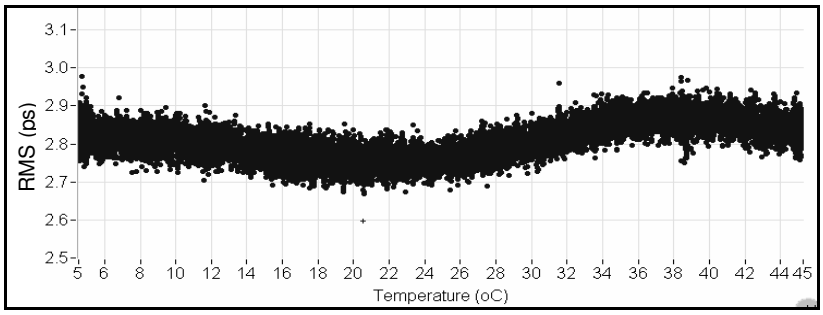


Figure 2. RMS error after re-calibrations with use of PLL synthesizer

As an alternative solution, it is possible to create preliminary calibration tables for different temperature ranges of the Riga ET operation, and automatically select one of the tables, taking into account the current internal temperature. Evident advantage of this approach is actual exclusion of the calibration as a complicated online operation. Practicability of this approach has been experimentally confirmed in Event Timer Module realization [*Artyukh Yu., et al.,* 2008]. It seems that, in combination with the right temperature compensation, this approach will allow to considerably improve precision characteristics of the Riga Event Timers.

2 More compact design and faster operating

Taking into account a performance of the modern super-high integration chips that have more and more integrated functions and provide higher operation speeds, it is possible to make the Riga ET design more compact, operating at higher frequencies, and having a faster interface with user tasks in PC.

In the A033-ET device the functions, associated with the control of measurement process in accordance with commands from PC, and the timing data recording into a buffer memory chip, are implemented in FPGA from Altera Corp. Now there are more complicated FPGAs containing a few millions of logic gates and a few millions bits of memory. This will allow to implement in FPGA all digital functions of the Riga ET, including:

- creating and supporting a large buffer memory,
- executing the calibration procedure and storing the interpolation tables,
- a clock pulses counting for time of event coarse fraction,
- providing the timer arming with a time of stop event prediction,
- managing the input signal conditioning and normalizing,
- a digital processing of ADC samples and event time-tag formation,
- processing the commands from and delivering timing data to user tasks in PC.

Implementation of timing related digital functions on single FPGA will allow to make the timer hardware more reliable and compact, with lower power consumption.

It seems attractive to increase the device internal clock frequency. Higher clock will allow to get better RMS resolution and shorter “dead time”, which are considered as the main performance characteristics of the event timers. But with higher clock the problem of logic competitions in ADC and FPGA can appear, so the alternative choice between speed and safety should be done.

PC interfaces with peripherals include a wide variety of types and performances. The most popular for measurement devices connection are: new USB3, providing data transfer at 400 Mbyte/s; PCI Express, having exchange speed from 250 Mbyte/s up to 1Gbyte/s; and Gigabit Ethernet – from 12 Mbyte/s up to 3Gbyte/s. Application of such high-speed interfaces will allow considerable increasing the average rate of continuous event timing and extending the control functionality from the user tasks. First attempt of function integration and performance increasing is realized in our Event Timer Module [*Artyukh Yu., et al.,* 2008*)*. This module, having the same RMS resolution 3-5 ps, is distinguished by compact size (130x110x20 mm), and faster USB2 interface.

3 User interface friendliness

The A033-ET operation is fully controlled by the ET-client via TCP/IP network or directly by a user program, which is built on the base of the sample program delivered with the A033-ET. To prepare the A033-ET for measurements the user executes the next procedures: calibration procedure to get an interpolation table; time synchronization with external GPS to get an offset of the ET time scale; and arming command sequence for certain measurement mode. After that the events coming at the inputs of the ET device are logged in the internal buffer memory and this timing information can be read into PC. To get the epoch time-tag in seconds for logged events the user reads from the ET device 8 bytes containing the number of hardware internal clock counts and ADC samples for each event, and converts these bytes to epoch in seconds, using the interpolation table and offset. If the ET gating mechanism is used it is necessary, on a base of the time of the Start event marked by a special flag, to calculate the time until Stop event and write this time back to the ET device.

To make the user interface with the Riga event timer friendlier, it is necessary minimize the volume of processing and the number of executed command. We plan to transfer some procedures, currently executed in PC, into hardware device, leaving to user only the main functions: start measurement in desired mode, and get directly the epoch time-tags expressed in seconds for all registered events.

Summary

Thus we have defined three main directions of further Riga Event Timer development, based on our view of SLR problems:

- the best and stable precision
- more compact and faster realization
- user interface friendliness

Some results are already achieved such as single-shot RMS resolution less than 3 ps, weakened dependence on temperature, robust calibration independents on temperature variation, and modular design with USB2 interface. All other tasks are planned for realization in the near future.

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